What is claimed is:

[Claim 1] 1. A semiconductor memory device comprising a bank with multiple pages, the device comprising means for keeping multiple pages open on the bank.

[Claim 2] 2. A semiconductor memory device according to claim 1, wherein the keeping means is operative to post a precharge command immediately after a command for a first access of one of the multiple pages in anticipation of a subsequent access of the page, the keeping means keeping the page open for a number of clock cycles and the precharge command causing a precharge operation to be executed after completion of the number of clock cycles.

[Claim 3] 3. A semiconductor memory device according to claim 2, further comprising means for resetting the keeping means if the subsequent access of the page occurs while the page is open, the resetting means operating to further delay execution of the precharge operation initiated by the precharge command.

[Claim 4] 4. A semiconductor memory device according to claim 1, wherein the bank comprises memory cells arranged in arrays of rows and columns, and the keeping means comprises a counter in a row path operatively connected to the rows of the bank.

[Claim 5] 5. A semiconductor memory device according to claim 1, wherein the keeping means comprises latches coupled to a sense amplifier associated with the bank, the latches operating in the storage of data read-from and written-to the sense amplifier.

[Claim 6] 6. A semiconductor memory device according to claim 1, wherein the device comprises a sense amplifier and a SRAM register coupled to the sense amplifier to provide low column access latency.

[Claim 7] 7. A semiconductor memory device according to claim 1, wherein bank comprises memory cells arranged in arrays of rows and columns, the memory cells comprise storage cells, and the storage cells comprise at least one transistor and at least one capacitor.

[Claim 8] 8. A semiconductor memory device according to claim 1, wherein the device has a dynamic random access memory architecture.

[Claim 9] 9. A semiconductor memory device according to claim 1, wherein the device is a nonvolatile memory device with multiple pages open in a block or sector thereof.

[Claim 10] 10. A semiconductor memory device according to claim 9, wherein the device is a flash memory device.

[Claim 11] 11. A semiconductor memory controller operable to issue commands to a memory module comprising multiple memory integrated circuits with memory cells arranged in arrays of rows and columns defining multiple pages, the memory controller comprising means for performing a posted precharge operation immediately after a command for a first access of a page in anticipation of a subsequent access of the page.

[Claim 12] 12. A semiconductor memory controller according to claim 11, wherein the performing means comprises a counter in a row path operatively connected to the rows of the memory cells.

[Claim 13] 13. A semiconductor memory controller according to claim 12, further comprising means for resetting the counter if the subsequent access of the page occurs while the page is open, the resetting means operating to further delay execution of the precharge operation.

[Claim 14] 14. A semiconductor memory controller according to claim 11, further comprising means for resetting the performing means if the subsequent access of the page occurs while the page is open, the resetting means operating to further delay execution of the precharge operation.

[Claim 15] 15. A semiconductor memory controller according to claim 11, wherein the performing means comprises latches coupled to sense amplifiers associated with the memory integrated circuits, the latches operating in the storage of data read-from and written-to the sense amplifiers.

[Claim 16] 16. A semiconductor memory controller according to claim 11, wherein the memory controller comprises sense amplifiers and a SRAM register coupled to the sense amplifiers to provide low column access latency.

[Claim 17] 17. A semiconductor memory controller according to claim 11, wherein the memory cells comprise storage cells, and each of the storage cells comprises at least one transistor and at least one capacitor.

[Claim 18] 18. A semiconductor memory controller according to claim 11, wherein the memory controller is a component of a dynamic random access memory architecture.

[Claim 19] 19. A semiconductor memory controller according to claim 11, wherein the memory controller is a component of a nonvolatile memory device with multiple pages open in a block or sector thereof.

[Claim 20] 20. A semiconductor memory controller according to claim 19, wherein the memory controller is a flash memory device.

[Claim 21] 21. A method comprising the step of keeping open more than one page of multiple pages on a bank of a semiconductor memory device.

[Claim 22] 22. A method according to claim 21, wherein the step comprises posting a precharge command immediately after a command for a first access of one of the multiple pages in anticipation of a subsequent access of the page.

[Claim 23] 23. A method according to claim 22, wherein the page is kept open for a number of clock cycles following the precharge command and the precharge command causes a precharge operation to be executed after completion of the number of clock cycles.

[Claim 24] 24. A method according to claim 23, further comprising the step of resetting the number of clock cycles if the subsequent access of the page occurs while the page is open, the resetting step operating to further delay execution of the precharge operation.

[Claim 25] 25. A method according to claim 22, wherein a precharge operation is initiated after the precharge command and following a delay determined by a counter.

[Claim 26] 26. A method according to claim 25, further comprising the step of resetting the counter so as to further delay the precharge operation if the subsequent access of the page occurs while the page is open.

[Claim 27] 27. A method according to claim 21, wherein the bank comprises memory cells arranged in arrays of rows and columns, and the precharge command is performed by a precharge counter that, when a row address is latched and a page is opened, the counter locks into the row address until reset, and when the precharge command is made, an internal activation for performing a precharge operation is activated after a predetermined number of clock cycles.